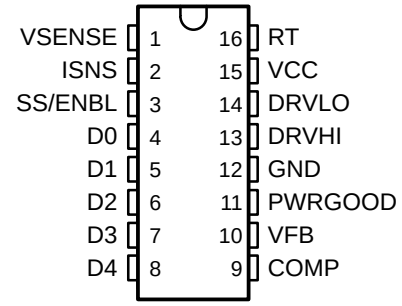
UCC3588
5-BIT PROGRAMMABLE OUTPUT BiCMOS POWER SUPPLY CONTROLLER

SLUS311A – JULY 1999 – REVISED AUGUST 2000

- **5-Bit Digital-to-Analog Converter (DAC) supports Intel Pentium II**
- **Microprocessor VID Codes**
- **Compatible with 5-V or 12-V Systems**
- **1% Output Voltage Accuracy Ensured**
- **Drives 2 N-Channel MOSFETs**
- **Programmable Frequency to 800 kHz**
- **Power Good OV / UV / OVP Voltage Monitor**
- **Undervoltage Lockout and Softstart Functions**
- **Short Circuit Protection**
- **Low Impedance MOSFET Drivers**
- **Chip Disable**

D, J, N AND PW PACKAGES
(TOP VIEW)



AVAILABLE OPTIONS

T_J	PACKAGED DEVICES			
	D, 16-PIN	J, 16-PIN	N, 16-PIN	PW, 16-PIN
0°C TO 70°C	UCC3588D	UCC3588J	UCC3588N	UCC3588PW

description

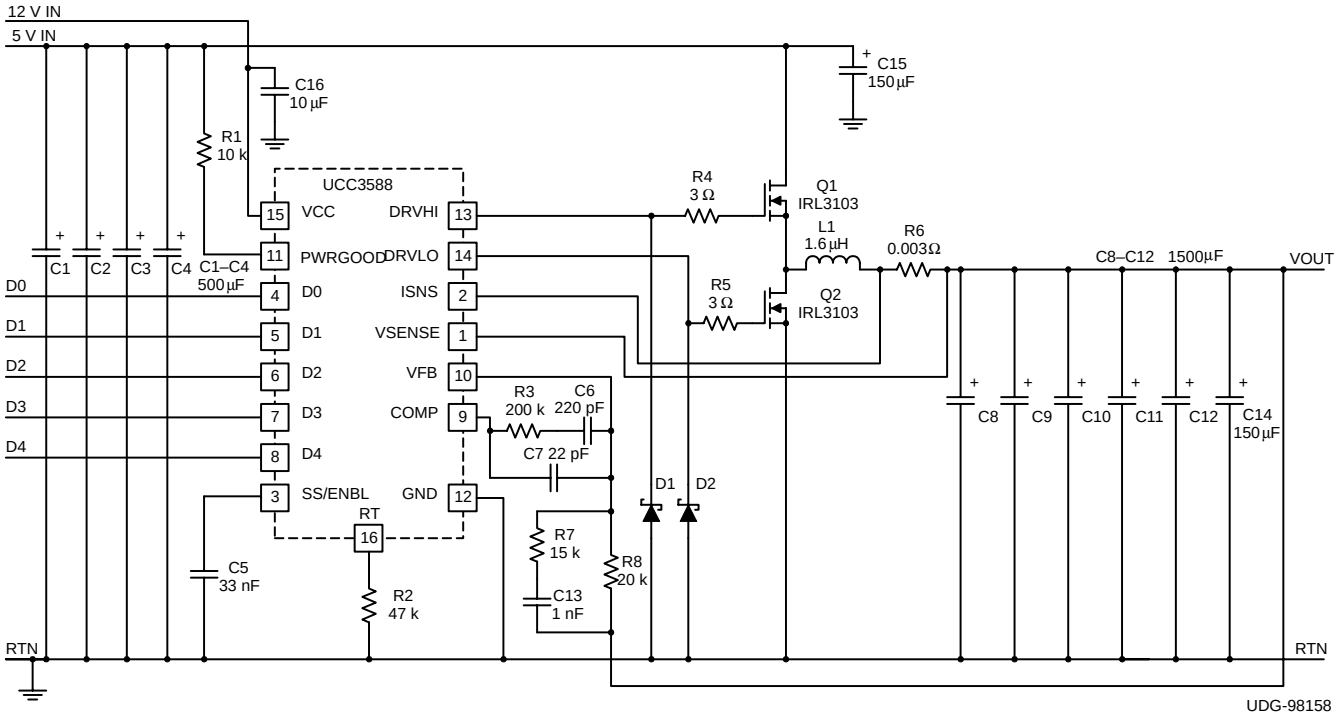
The UCC3588 synchronous step-down (Buck) regulator provides accurate high efficiency power conversion. Using few external components, the UCC1588 converts 5V to an adjustable output ranging from 3.5 VDC to 2.1 VDC in 100-mV steps and 2.05 VDC to 1.3 VDC in 50-mV steps with 1% dc system accuracy. A high level of integration and novel design allow this 16-pin controller to provide a complete control solution for today's demanding microcontroller power requirements. Typical applications include on board or VRM based power conversion for Intel Pentium II microprocessors, as well as other processors from a variety of manufacturers. High efficiency is obtained through the use of synchronous rectification.

The softstart function provides a controlled ramp up of the system output voltage. Overcurrent circuitry detects a hard (or soft) short on the system output voltage and invokes a timed softstart/shutdown cycle to reduce the PWM controller on time to 5%.

The oscillator frequency is externally programmed with RT and operates over a range of 50 kHz to 800 kHz. The gate drivers are low impedance totem pole output stages capable of driving large external MOSFETs. Cross conduction is eliminated by fixed delay times between turn off and turn on of the external high side and synchronous MOSFETs. The chip includes undervoltage lockout circuitry which assures the correct logic states at the outputs during power up and power down.

This device is available in 16-pin surface mount, plastic and ceramic DIP, and TSSOP packages. The UCC3588 is specified for operation from 0°C to 70°C.

application diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage V_{CC} . . . . . 15 V
Gate drive current, 50% duty cycle . . . . . 1 A
Input voltage, V_{SENSE}, V_{FB}, SS, COMMAND, COMP . . . . . 5 V
Input voltage, D0, D1, D2, D3, D4 . . . . . 6 V
Input current, RT, COMP . . . . . 5 mA

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

thermal data

Plastic DIP package,
thermal resistance junction to leads, Θjc . . . . . 45°C/W
thermal resistance junction to ambient, Θja . . . . . 90°C/W

Ceramic DIP package,
thermal resistance junction to leads, Θjc . . . . . 28°C/W
thermal resistance junction to ambient, Θja . . . . . 120°C/W

Standard surface mount package,
thermal resistance junction to leads, Θjc . . . . . 35°C/W
thermal resistance junction to ambient, Θja . . . . . 120°C/W

NOTE The above numbers for Θja and Θjc are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The Θja numbers are meant to be guidelines for the thermal performance of the device and PC board system. All of the above numbers assume no ambient airflow, see the packaging section of Unitrode Product Data Handbook for more details.

electrical characteristics, T_A = 0°C to 70°C. $T_A = T_J$. V_{CC} = 12 V, RT = 49 k, (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Supply current, on	V_{CC} = 12 V, V_{RT} = 2 V		4.5	5.5	mA
UVLO Section					
VCC UVLO turnon threshold		10.05	10.50	10.85	V
UVLO threshold hysteresis		350	450	550	mV
Voltage Error Amplifier Section					
Input bias current	V_{CM} = 2.0 V		–0.025	–0.050	mA
Open loop gain	See Note 5		77		dB
Output voltage high	I_{COMP} = –500 mA	3.5	3.6		V
Output voltage low	I_{COMP} = 500 mA		0.2	0.5	V
Output source current	V_{VFB} = 2 V, VCOMMAND = V_{COMP} = 2.5 V	–400	–500		mA
Output sink current	V_{VFB} = 3 V, VCOMMAND = V_{COMP} = 2.5 V	5	10		mA
Oscillator/PWM Section					
Initial accuracy	0°C < T_A < 70°C	250	270	290	kHz
Ramp amplitude (p–p)			1.85		V
Ramp valley voltage			0.65		V
PWM max duty cycle	COMP = 3 V See Note 5		100		%
PWM min duty cycle	COMP = 0. 3 V See Note 5		0		%
PWM delay to outputs (high to low)	COMP = 1.5 V See Note 5		150		ns
PWM delay to outputs (low to high)	COMP = 1.5 V See Note 5		150		ns
Transient Window Comparator Section					
Detection range high (duty cycle = 0)	% Over $V_{COMMAND}$, See Note 1		3		%
Detection range low (duty cycle = 1)	% Under $V_{COMMAND}$, See Note 1		–3		%
Propagation delay (V_{SENSE} to outputs)			150	200	nS
Soft Start/ Shutdown Section					
SS charge current (normal start-up)	Measured on SS	–6		–12	mA
SS charge current (short circuit fault condition)	Measured on SS	–60	–100	–120	mA
SS discharge current (during timeout sequence)	Measured on SS	1	2.5	5	mA
Shutdown threshold	Measured on SS	4.1	4.2	4.3	V
Restart threshold	Measured on SS	0.4	0.5	0.6	V
Soft start complete threshold (normal start–up)	Measured on SS	3.5	3.7	3.9	V

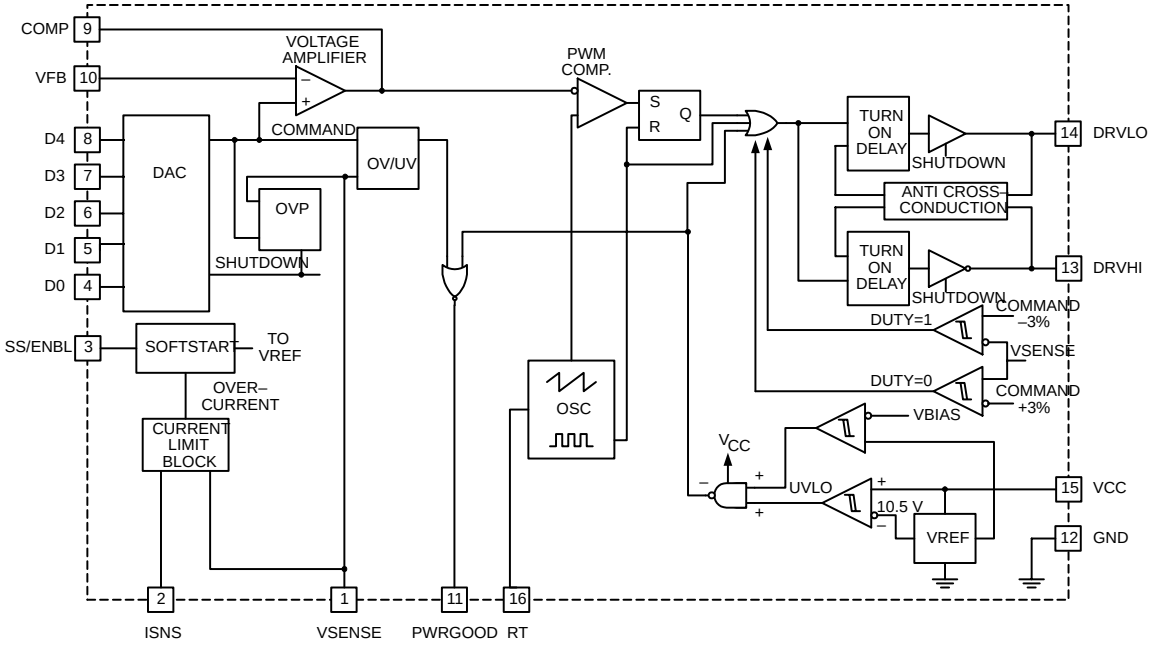
NOTES:
1. This percentage is measured with respect to the ideal command voltage programmed by the V_{ID} (D0,....,D4) pins and applies to all DAC codes from 1.3 V to 3.5 V.
2. Reference and error amplifier offset trimmed while the voltage amplifier is set in unity gain mode.
3. Deadtime delay is measured from the 50% point of DRVHI falling to the 50% point of DRVLO rising, and vice-verse.
4. This time is dependent on the value of C_{SS}.
5. Ensured by design. Not 100% production tested.

electrical characteristics, T_A = 0°C to 70°C. $T_A = T_J$. V_{CC} = 12 V, RT = 49 k, (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC / Reference Section					
COMMAND voltage accuracy	10.8 V < V_{CC} < 13.2 V, measured on COMP, 0°C < T_A < 70°C, See Note 2	–1.0		1.0	%
D0 to D4 voltage high		5.5	6	6.5	V
D0 to D4 voltage threshold		2.5	3.0	3.5	V
D0 to D4 voltage input bias current	V(D4,...,D0) < 0.5 V	–80	–100		mA
Overvoltage Comparator Section					
Trip point	% Over $V_{COMMAND}$, See Note 1	8		12	%
Hysteresis		10	20	35	mV
Undervoltage Comparator Section					
Trip point	% Under $V_{COMMAND}$, See Note 1	–8.0		–12.0	%
Hysteresis		10	20	35	mV
PWRGOOD Signal Section					
Output impedance	V_{CC} = 12 V, $I_{PWRGOOD}$ = 1 mA			470	W
Overvoltage Protection Section					
Trip point	% Over $V_{COMMAND}$, See Note 1	15	17.5	20	%
Hysteresis			20	35	mV
VSENSE input bias current	OV, OVP, UV combined	–8	–12	–16	mA
Gate Drivers (DRVHI, DRVLO) Section					
Output high voltage	I_{GATE} = 100 mA, V_{CC} = 12 V	10.8	11.5		V
Output low voltage	I_{GATE} =–100 mA, V_{CC} = 12 V		0.5	0.8	V
Driver non-overlap time (DRVHI– to DRVLO+)	See Note 3	90	120	150	ns
Driver non-overlap time (DRVLO– to DRVHI+)	See Note 3	50	80	120	ns
Driver rise time	3 nF capacitive load		80	100	ns
Driver fall time	3 nF capacitive load		80	100	ns
Current Limit Section					
Start of quick charge to shutdown threshold	V_{ISNS} = V_{SENSE} + 75 mV, C_{SS} = 10 nF, See Note 4, See Note 5		50		ms
Current limit threshold voltage	$V_{THRESHOLD}$ = V_{ISNS} – V_{VSENSE}	40	54	70	mV
ISNS input bias current		–8	–12	–16	mA

NOTES: 6. This percentage is measured with respect to the ideal command voltage programmed by the V_{ID} (D0,....,D4) pins and applies to all DAC codes from 1.3 V to 3.5 V.
7. Reference and error amplifier offset trimmed while the voltage amplifier is set in unity gain mode.
8. Deadtime delay is measured from the 50% point of DRVHI falling to the 50% point of DRVLO rising, and vice-verse.
9. This time is dependent on the value of C_{SS}.
10. Ensured by design. Not 100% production tested.

block diagram



pin assignments

COMP: (Voltage Amplifier Output) The system voltage compensation network is applied between COMP and VFB.

D0, D1, D2, D3, D4: These are the digital input control codes for the DAC. The DAC is comprised of two ranges set by D4, with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB). A bit is set low by being connected the pin to GND; a bit is set high by floating the pin. Each control pin is pulled up to approximately 6 V by an internal pull-up. If one of the low voltage codes is commanded on the DAC inputs, the outputs will be disabled. The outputs will also be disabled for all 1's, the NO CPU command.

DRVHI: (PWM Output, MOSFET Driver) This output provides a low Impedance totem-pole driver. Use a series resistor between this pin and the gate of the external MOSFET to prevent excessive overshoot. Minimize circuit trace length to prevent DRVHI from ringing below GND. DRVHI is disabled during UVLO conditions. DRVHI has a typical output impedance of 5 Ω for a V_{CC} voltage of 12 V.

DRVLO: (synchronous rectifier output, MOSFET driver) This output provides a low Impedance totem-pole driver to drive the low-side synchronous external MOSFET. Use a series resistor between this pin and the gate of the external MOSFET to prevent excessive overshoot. Minimize circuit trace length to prevent DRVLO from ringing below GND. DRVLO is disabled during UVLO conditions. DRVLO has a typical output impedance of 5 Ω for a V_{CC} voltage of 12 V.

GND: (Ground) All voltages measured with respect to ground. V_{CC} should be bypassed directly to GND with a 0.1-µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing to GND should be as short and direct as possible.

ISNS: (Current Limit Sense Input) A resistance connected between this sense connection and V_{SENSE} sets up the current limit threshold (54-mV typical voltage threshold).

PWRGOOD: This pin is an open drain output which is driven low to reset the microprocessor when VSNS rises above or falls below its nominal value by 8.5%(typ). The on resistance of the open-drain switch is no higher than 470 Ω. This output should be pulled up to a logic level voltage and should be programmed to sink 1 mA or less.

pin assignments (continued)

RT: (Oscillator Charging Current) This pin is a low impedance voltage source set at ~1.25 V. A resistor from RT to GND is used to program the internal PWM oscillator frequency. The equation for R_T follows:

$$R_T = \left(\frac{1}{(f \times 67.2\ pF)}\right) - 800 \quad (1)$$

SS/ENBL: (Soft Start/Shut Down) A low leakage capacitor connected between SS and GND will provide a softstart function for the converter. The voltage on this capacitor will slowly charge on start-up via an internal current source (10 mA typ.) and ultimately clamp at approximately 3.7 V. The output of the voltage error amplifier (COMP) tracks this voltage thereby limiting the controller duty ratio. If a short circuit is detected, the clamp is released and the cap on SS charges with a 100 mA (typ) current source. If the SS voltage exceeds 4.2 V, the converter shuts down, and the 100-mA current source is switched off. The SS cap will then be discharged with a 2.5-mA (typ) current sink. When the voltage on SS falls below 0.5 V, a new SS cycle is started. The equation for softstart time follows:

$$T_{SS} = 3.7\left(\frac{C_{SS}}{10\ \mu A}\right) \quad (2)$$

Shutdown is accomplished by pulling SS/SD below 0.5 V.

VCC: (Positive Supply Voltage) This pin is normally connected to a 12-V ±10% system voltage. The UCC1588 will commence normal operation when the voltage on VCC exceeds 10.5 V (typ). Bypass VCC directly to GND with a 0.1-µF (minimum) ceramic capacitor to supply current spikes required to charge external MOSFET gate capacitances.

VFB: (Voltage Amplifier Inverting Input) This is normally connected to a compensation network and to the power converter output through a divider network.

VSENSE: (Direct Output Voltage Connection) This pin is a direct kelvin connection to the output voltage used for over voltage, under voltage, and current sensing.

APPLICATION INFORMATION

Figure 1 shows a synchronous regulator using the UCC3588. It accepts 5 V and 12 V as input, and delivers a regulated dc output voltage. The value of the output voltage is programmable via a 5-bit DAC code to a value between 1.3 V and 3.5 V. The example given here is for a 12-A regulator, running from a 10% tolerance source, and operating at 300 kHz.

The design of the power stage is straightforward buck regulator design. Assuming an output noise requirement of 50 mV, and an output ripple current of 20% of full load, the value of the output inductor should be calculated at the highest input voltage and lowest output voltage that the regulator is likely to see. This insures that the ripple current will decrease as the input voltage and output voltage differential decreases. The minimum duty cycle, dmin, should also be calculated under this condition.

1) The current sense resistor is chosen to allow current limit to occur at 1.4 times the full load current.

$$R6 = \frac{V_{TRIP}}{\left(1.4 \times I_{OUT}\right)} = \frac{50\ mV}{16.8\ A} = 3\ m\Omega \quad (3)$$

APPLICATION INFORMATION

2) To properly approximate the full load duty cycle operating range, assumptions are made regarding the MOSFETs' $R_{DS(on)}$, and the output inductor's dc resistance. Q1 and Q2 are IRF3103s, each with an $R_{DS(on)}$ of 0.014 Ω. The output inductor is allowed to dissipate one watt under full load, giving a dc resistance of 6.9 mW, and R6 is 3 mΩ. The resulting duty cycle at the operating extremes is then:

$$\delta_{MIN} = \frac{V_{OUT(IO)} + I_{OUT} \times \left(R6 + R_{DS(on)} + R\ell\right)}{V_{IN(HI)}} = \frac{1.8 + (12 \times 0.024)}{5.5} = 0.379 \quad (4)$$

$$\delta_{MIN} = \frac{V_{OUT(HI)} + I_{OUT} \times \left(R6 + R_{DS(on)} + R\ell\right)}{V_{IN(LO)}} = \frac{3.5 + (12 \times 0.024)}{4.5} = 0.842 \quad (5)$$

3) The value of the output inductor is chosen at the worst case ripple current point.

$$L = \frac{\left(V_{IN(HI)} - V_{OUT(LO)}\right)}{\Delta V_{OUT}} = \frac{(5.5 - 1.8) \times 0.379 \times 3.333\,\mu}{2.4} = 1.9\ \mu H \quad (6)$$

Four turns of #16 on a micrometals T51-52C core has an inductance of 1.9 μH, has a dc resistance of 6.6 mΩ, and will dissipate about 1 W under full load conditions. With an output inductor value of 1.9 μH, the ripple current will be 1750 mA under the low-input-high-output condition.

4) To meet the output noise voltage requirement, the output capacitor(s) must be chosen so that the ripple voltage induced across the ESR of the capacitors by the output ripple current is less than 50 mV.

$$ESR < \frac{50\ mV}{\Delta I_{OUT}} = 42\ m\Omega \quad (7)$$

Additionally, to meet output load transient response requirements, the capacitors' ESL and ESR must be low enough to avoid excessive voltage transient spikes. (See Application Note U-157 for a discussion of how to determine the amount and type of load capacitance.) For this example, four Sanyo MV-GX 1500-μF, 6.3-V capacitors will be used. The ESR of each capacitor is approximately 44 mΩ so the parallel combination of four results in an equivalent ESR of 11 mΩ.

5) Q1 and Q2 are chosen to be IRF3103 N-Channel MOSFETs. Each MOSFET has an $R_{DS(on)}$ of approximately 0.014 Ω, a gate charge requirement of 50 nC, and a turn-off time of approximately 54 ns.

To calculate the losses in the upper MOSFET, Q1, first calculate the RMS current it will be conducting.

$$I\left(Q1_{RMS}\right) = \sqrt{\delta\left[I_{OUT}{}^2 + \frac{\Delta I_{OUT}{}^2}{12}\right]} \quad (8)$$

Notice that with a higher output voltage, the duty cycle increases, and therefore so does the RMS current. Any heat sink design should take into account the worst case power dissipation the device will experience.

APPLICATION INFORMATION

With the highest programmable output voltage of 3.5 V and the lowest possible input voltage of 4.5 V, the RMS current Q1 will conduct is 10.5 A, and the conduction loss is:

$$P_{CON}Q1 = \left(I_{Q1_{RMS}}\right)^2 \times R_{DS(on)} = 1.5\ W \tag{9}$$

Next, the gate drive losses are found.

$$P_{CON}Q1 = Q_G \times f_S = 0.08\ W \tag{10}$$

And the turn-off losses are estimated as

$$P_{T(OFF)}Q1 = \frac{1}{2}V_{IN(HI)} \times I_{D(PK)} \times tf \times F_S = 0.56\ W \tag{11}$$

The total loss in Q1is the sum of the three components, or about 2.1 W.

The gate drive losses in Q2 will be the same as in Q1, but the turn-off losses will be associated with the reverse recovery of the body diode, instead of the turn-off of the channel. This is due to the UCC3588's delay built into the switching of the upper and lower MOSFET's drive. For example, when Q1 is turned-off, the turn-on of Q2 is delayed for about 100 ns, insuring that the circuit has time to commutate and that current has begun to flow in the body diode of Q2. When Q2 is turned-off, current is diverted from the channel of Q2 into the body diode of Q2, resulting in virtually no power dissipation. When Q1 is turned ON 100ns later however, the circuit is forced to commutate again. This time causing reverse recovery loss in the body diode of Q2 as its polarity is reversed. The loss in the diode is expressed as:

$$P_{RR}Q2 = \frac{1}{2} \times Q_{RR} \times V_{IN(HI)} \times F_S = 0.26\ W \tag{12}$$

Where Q_{RR}, the reverse recovery of the body diode, is 310 nC.

100 ns before the turn-on of Q2, and 100 ns after the turn-off of Q2, current flows through Q2's intrinsic body diode. The power dissipation during this interval is:

$$P_{COM}Q2_{DIODE} = I_{OUT} \times V_{DIODE} \times \frac{200\ ns}{3.33\ \mu s} = 12 \times 1.4 \times 0.06 = 1\ W \tag{13}$$

During the ON period of Q2, current flows through the $R_{DS(on)}$ of the device. Where the highest RMS current in Q1 was at the low-input and high-output condition, the highest RMS current in Q2 is found when the input is at its highest, and the output is at its lowest. The equation for the RMS current in Q2 is:

$$I\left(Q2_{RMS}\right) = \sqrt{\left(1 - \delta_{MIN} - \frac{200\ ns}{3.33\ \mu s}\right) \times \left[I_{OUT}^{\ 2} + \Delta\frac{I_{OUT}^{\ 2}}{12}\right]} = 8.7\ A \tag{14}$$

$$P_{CON}Q2 = 1\left(Q2_{RMS}^{\ 2}\right) \times R_{DS(on)} = 1.06\ W \tag{15}$$

The worst case loss in Q2 comes to about 2.4 W.

APPLICATION INFORMATION

6) Repeating the preceding procedure for various input and output voltage combinations yields a table of operating conditions.

Table 1. Regulator Operating Conditions

	VIN=		
	4.5	**5.0**	**5.5**
VOUT = 3.5			
Pd Q1	2.20	2.10	2.00
Pd Q2	1.50	1.60	1.80
Pd L	0.95	0.95	0.95
Pd total	5.10	5.20	5.40
Average input	10.5	9.50	8.70
Duty cycle	0.84	0.76	0.69
VOUT = 1.8			
Pd Q1	1.5	1.40	1.40
Pd Q2	2.3	2.40	2.50
Pd L	0.95	0.95	0.95
Pd total	5.2	5.30	5.40
Average input	6.00	5.40	4.96
Duty cycle	0.46	0.42	0.38

7) Assuming the converter's input current is dc, the remaining switching current drawn by Q1 must come from the input capacitors. The next step then, is to find the worst case RMS current the capacitors will experience. (Equation 16). Where $I_{IN(avg)}$ is the average input current.

$$I_{CAP_{RMS}} = \sqrt{\delta\left[\left(I_{OUT} - I_{IN(avg)}\right)^2 + \frac{\Delta I_{OUT}^2}{12}\right] + (1 - \delta) \times \left(I_{IN(avg)}\right)^2} \quad (16)$$

Repeating the above calculation over the operating range of the regulator (see Table 2.) reveals that the worst case capacitor ripple current is found at low input, and at low output voltage. A Sanyo MV-GX, 1500-µF, 6.3-V capacitor is rated to handle 1.25 A at 105°C. Derating the design to 70°C allows the use of four capacitors, each one experiencing one fourth of the total ripple current.

8) The voltage feedback loop is next. The gain and frequency response of the PWM and LC filter is shown in Equation 17.

$$K_{PWM}(f) = \frac{V_{IN}}{V_{RAMP}} = \quad (17)$$

$$\frac{1 + 2\pi f \times R_{ESR} \times C_{OUT}}{1 - \left(4\pi^2 \times f^2 \times LC_{OUT}\right) + \left(\left(R6 + R\ell + R_{ESR}\right) \times C_{OUT} + \frac{L}{R_{LOAD}}\right)}$$

APPLICATION INFORMATION

Table 2. Regulator Operating Conditions

	VIN=		
	4.5	**5.0**	**5.5**
VOUT=3.5			
Total input cap RMS current	4.40	5.20	5.60
Total input cap power dissipation	0.21	0.29	0.34
Total power dissipation	5.10	5.30	5.40
Power train efficiency	0.89	0.88	0.87
VOUT=1.8			
Total input cap RMS current	6.00	5.90	5.80
Total input cap power dissipation	0.39	0.39	0.37
Total power dissipation	5.20	5.30	5.40
Power train efficiency	0.81	0.80	0.80

GAIN vs FREQUENCY

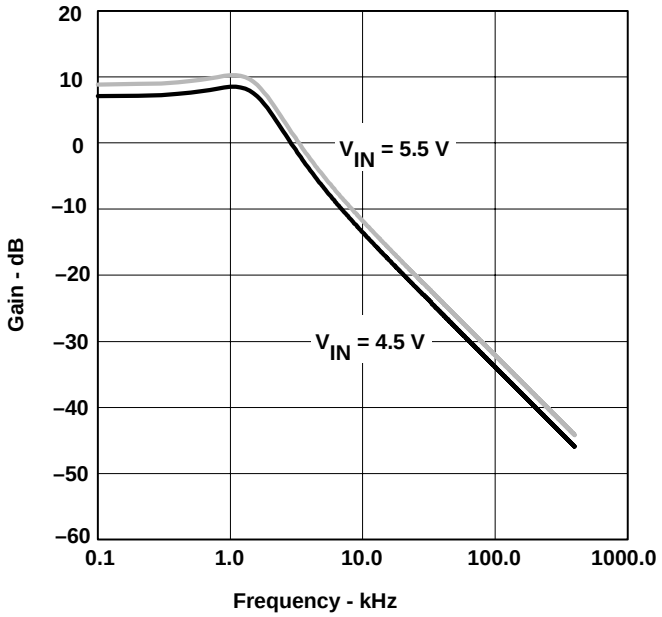


Figure 1

PHASE vs FREQUENCY

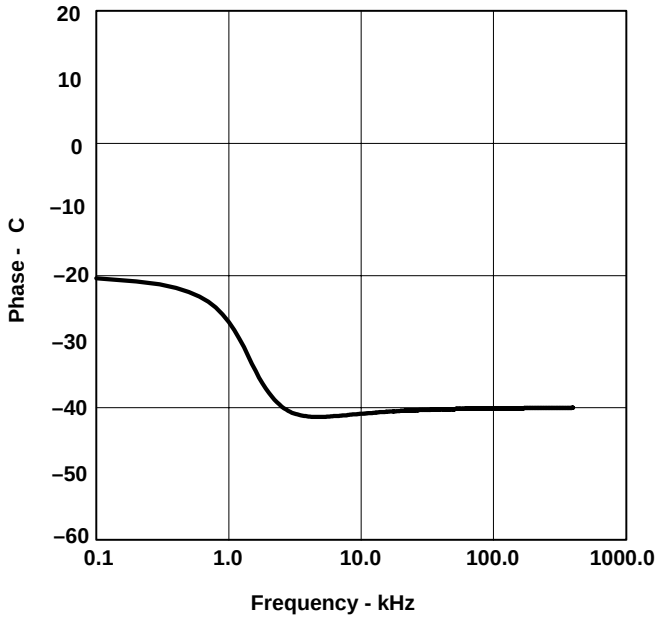


Figure 2

To compensate the loop with as high a bandwidth as practical, additional gain is added to the loop with the voltage error amplifier.

APPLICATION INFORMATION

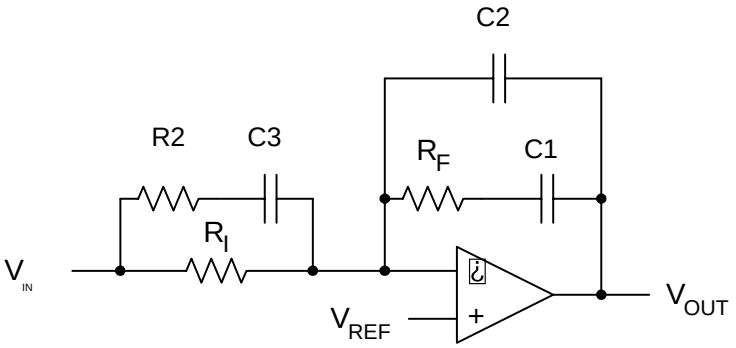


Figure 3. Voltage Error Amplifier Configuration

The equation for the gain of the voltage amplifier in this configuration is:

$$K_{EA} = \frac{(1 + s(C1Rf)) \times \left(1 + s\left(C3\left(R_I + R2\right)\right)\right)}{R_I\left(s^2C1C2Rf + s(C1 + C2)\right) \times (1 + s(C3R2))} \quad (18)$$

For good transient response, select the RF-C1 zero at 5 kHz. Add additional phase margin by placing the RI-C3 zero also at 5 kHz. To roll off the gain at high frequency, selece the R2-C3 pole to be at 10 kHz, and the final C2-RF pole at 40 kHz. Results are RI = 20 k, RF = 200 k, R2 = 15 k, C1 = 220 pF, C2 = 20 pF, C3 = 1000 pF. The Gain - phase plots of the voltage error amplifier and the overall loop are plotted below.

9) The value of RT is given by:

$$RT = \left(\frac{1}{F_S} \times 67.2\ pF\right) - 800 = 48\ k\Omega \quad (19)$$

10) The value of the soft start capacitor is given by:

$$C_{SS} = 10\ \mu \times \frac{t_{SS}}{3.7}\ V \quad (20)$$

Where t_{SS} is the desired soft start time.

To insure that soft start is long enough so that the converter does not enter current limit during startup, the minimum value of soft start may be determined by:

$$C_{SS} \geq \frac{C_{OUT} \times I_{CH}}{\left(\frac{V_{LIM}}{R_{SENSE}}\right) - I_{OUT}} \times \frac{V_{IN}}{V_{RAMP}} \quad (21)$$

Where C_{OUT} is the output capacitance, Ich is the soft start charging current (10 mA typ), V_{LIM} is the current limit trip voltage (54 mV typ), I_{OUT} is the load current, V_{IN} is the 5-V supply, and V_{RAMP} is the internal oscillator ramp voltage (1.85 V typ). For this example, C_{SS} must be greater than 35 nF, and the resulting soft start time will be 13 ms.

APPLICATION INFORMATION

11) The output of the regulator is adjustable by programming the following codes into the D0 - D4 pins according to the table below. To program a logic zero, ground the pin. To program a logic 1, then leave the pin floating. Do not tie the pin to an external voltage source.

12) A series resistor should be placed in series with the gate of each MOSFET to prevent excessive ringing due to parasitic effects. A value of 3 Ω to 5 Ω is usually sufficient in most cases. Additionally, to prevent pins 13 and 14 from ringing more than 0.5-V below ground, a clamp schottky rectifier placed as close as possible to the IC is also recommended.

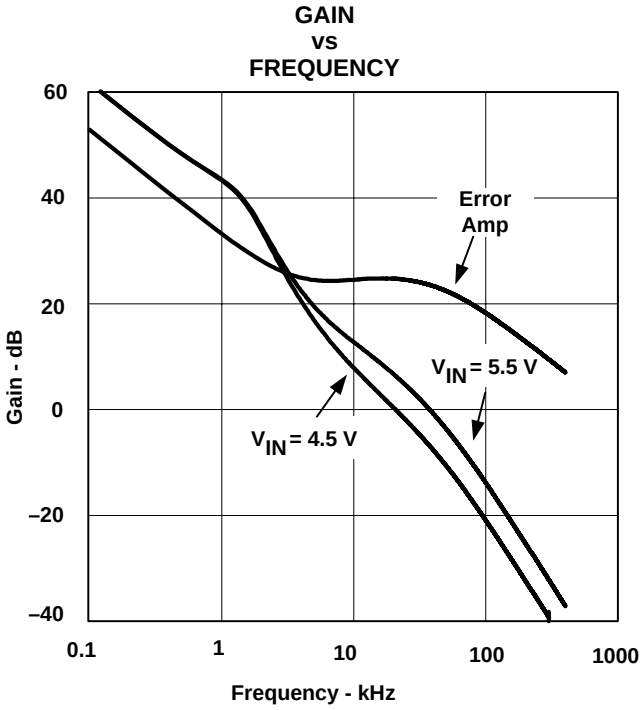


Figure 4

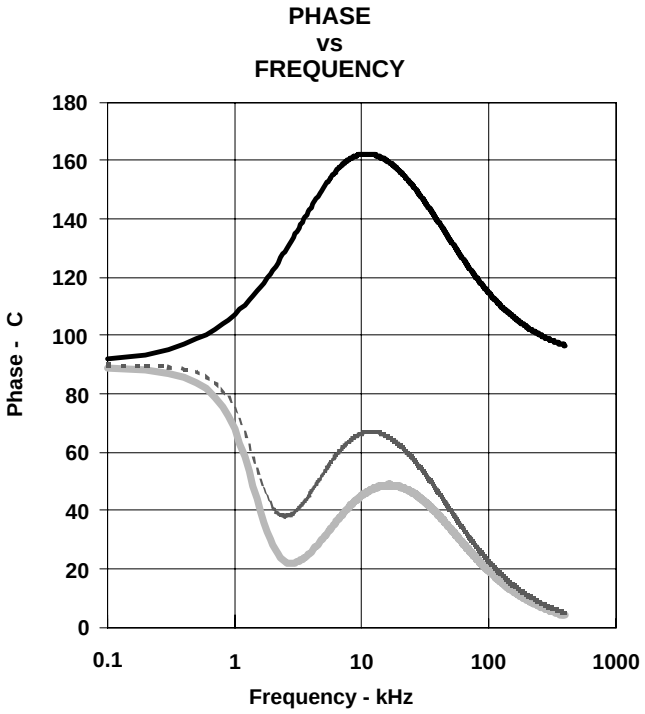


Figure 5

APPLICATION INFORMATION

Table 3. VID Codes and Resulting Regulator Output Voltage

D4	D3	D2	D1	D0	V_{OUT}
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05
1	1	1	1	1	No out-puts
1	1	1	1	0	2.10
1	1	1	0	1	2.20
1	1	1	0	0	2.30
1	1	0	1	1	2.40
1	1	0	1	0	2.50
1	1	0	0	1	2.60
1	1	0	0	0	2.70
1	0	1	1	1	2.80
1	0	1	1	0	2.90
1	0	1	0	1	3.00
1	0	1	0	0	3.10
1	0	0	1	1	3.20
1	0	0	1	0	3.30
1	0	0	0	1	3.40
1	0	0	0	0	3.50

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC3588D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
UCC3588DG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
UCC3588PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI
UCC3588PWG4	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI
UCC3588PWTR	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI
UCC3588PWTRG4	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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